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LINEARITY RESTRICTIONS FOR A CLASS OF PHASE FREQUENCY DETECTORS

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Abstract. In this paper, the transfer characteristic of a class of phase frequency detectors is analysed and modelled for simulations. It is demonstrated that the reasons of non-linearity of the transfer characteristic may originate both from the charge pump and the logic control unit of the phase frequency detector. Restricted slew rate is found to be one of the main reasons of non-linearity of the charge pump, determining the minimum duration of control signals. For a generalized structure of the control unit, an optimum distribution of gate delays is proposed. Also, some critical aspects of selecting the delays are considered which may cause significant non-linearity with a dead zone and even oscillation of the phase frequency detector. The results of the analysis are verified by transistor level SPICE simulation.

Key words: phase frequency detector, charge pump, gate delay, transfer characteristic, dead zone.

1. INTRODUCTION

In phase locked loop (PLL) structures, particularly in frequency synthesizers (FS), a phase frequency detector (PFD) is often used instead of the conventional phase detector (PD) [1–5]. Compared with the PD, the PFD has both the phase and the frequency sensitivity and an input range up to $\pm 2\pi$, which enables increasing of the acquisition range and locking speed of the tracking system.

In practice, some substantial problems arise by implementation of the PFD, such as non-linearity of the dynamic transfer characteristic (TC) and dc offset of the output signal. Mainly, the non-linearity is caused by the finite speed (time delays) of the components used (dynamic errors) as well as by tolerances and mismatching of the component parameters (static errors). In some cases, the gain of the PFD near zero crossing of the TC reduces below the critical level and a so-

called dead zone (DZ) appears, inducing excessive phase noise and instability of the FS output frequency [4].

In this paper, the main reasons of the inadequate behaviour of the PFD are analysed and described mathematically. It enables us to compose an improved model of the PFD for the PLL, particularly, for the FS analysis and simulations. Accounting for the actual propagation delays and slew rates of the components is especially important for high frequency applications, where the delays are comparable with the signal period. Also, some recommendations for improving the TC by means of parametrical as well as structural modification of the PFD are presented.

2. MAIN STRUCTURE OF THE PFD

The structure of a common class of the PFDs is presented in Fig. 1. The PFD converts the time delay between the active edges of the logic input signals into an analogue (current) signal, the average value of which is approximately proportional to the delay. It consists of a logic control unit (CU) with input signals V_{inp} and V_{inn} and output signals V_{up} and V_{dn} respectively, and a charge pump (CP), controlled by the CU, which generates output current pulses I_{cp}. While being the structural part of a PLL FS, the PFD output signal is processed by a low-pass filter (LPF), which removes the ripple, corrects the PLL dynamic, and produces a voltage signal for steering the voltage controlled oscillator (VCO). The latter generates an output signal with required (synthesized) frequency. The VCO output is connected to the (feedback) input of the CU through a frequency divider.

In classical approach [1–5], the CU of a duty cycle insensitive PFD includes two flip-flops and some logic gates. One of them is used to form a reset signal (RS) for the flip-flops [2,3], if both the control signals V_{up} and V_{dn} become active simultaneously. Typical (generalized) structure of the CU, often used in PFD, is presented in Fig. 2.

To improve the transfer performance of the CU, different schematic solutions have been proposed. Mostly, they are based on the classical structure [6,7], but also some novel structures have been designed. In [8], a structure based on the four RS-flip-flops is introduced. A simple DZ-free, but duty cycle sensitive structure is proposed in [9]. To correct timing of the output pulses and to remove

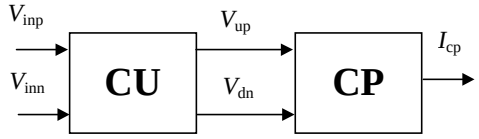

Fig. 1. General structure of the phase frequency detector.

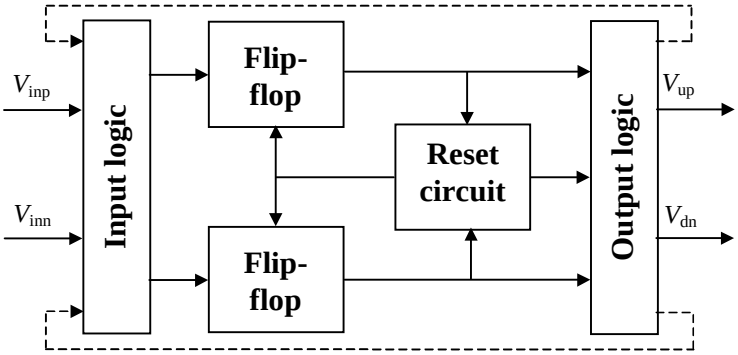

Fig. 2. Generalized structure of the control unit.

the DZ, additional delay elements are often introduced [10,11]. A more detailed description of a particular CU structure will be described in Chapter 4.

Simplified structure of the CP along with a LPF at its output is shown in Fig. 3. To speed up the current switching process, it is reasonable to keep the current source (sink) output at a particular voltage level V_0 (for instance, at $V_{\text{supply}}/2$). This avoids large voltage deviations at the CP output, causing re-charge of parasitic capacitance or saturation of transistors. Here, double switches can be used (shown by dashed lines in Fig. 3 [12]).

The averaged output current $I_{\text{cp,av}}$ of the CP can be considered as the output signal of the PFD, determined by the time (phase) difference Δt_{in} between the active ramps of input signals V_{inp} and V_{inn}. Hence, the TC of the PFD, CU and CP can be expressed as

$$I_{\text{cp,av}} = \text{f}_{\text{pfd}}(\Delta t_{\text{in}}), \quad \Delta t_{\text{cp}} = \text{f}_{\text{cu}}(\Delta t_{\text{in}}), \quad I_{\text{cp,av}} = \text{f}_{\text{cp}}(\Delta t_{\text{cp}}), \tag{1}$$

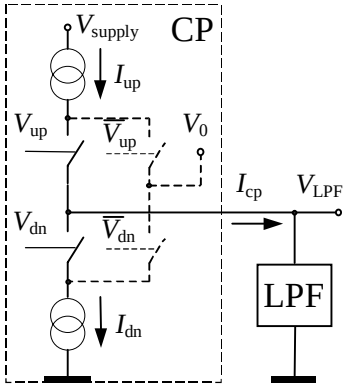

Fig. 3. Charge pump with the low-pass filter.

where Δt_{cp} is difference between the (normalized) duration of the pulses V_{up} and V_{dn}. All the delays and transient times of the components are considered as relative to the period T of synchronized input signals.

At a given value of the input variable, Δt_{in}, the TCs of the CU and CP can be characterized by their differential gains $K_{cu} = \mathrm{d}\Delta t_{cp} / \mathrm{d}\Delta t_{in}$ and $K_{cp} = \mathrm{d}I_{cp,av} / \mathrm{d}\Delta t_{cp}$, while the gain of the PFD expresses as $K_{pfd} = K_{cu} K_{cp}$. For approximately linear TCs of blocks, the gains of blocks and of the PFD are almost independent of the input value.

3. CHARGE PUMP

3.1. Transfer characteristic at balanced output

For simplifying the analysis of the CP, let us assume a symmetrical CU with output (control) pulses V_{up} and V_{dn}, having a minimum (active) duration of τ_{del}. Supposing that the V_{inp} is leading and V_{inn} is lagging, and assuming a linear CU with $K_{cu} = 1$ and $\Delta t_{cp} = \Delta t_{in}$, the shorter signal V_{dn} has relative duration (width) of $t_{dn} = \tau_{del}$, while the longer signal V_{up} has relative duration of $t_{up} = \tau_{del} + |\Delta t_{in}|$. At $\Delta t_{in} = 0$, both control pulses have the same minimum width τ_{del}. Also, an input threshold for the CP for control signals as a half of the "high" level value, and a constant slew rate $k_r = T\mathrm{d}I/\mathrm{d}t$ of the CP current source and sink are assumed. Then the relative transient time for the CP current pulses can be determined as $\tau_{cp} = I_n / k_r$, where I_n is the nominal current of the source and sink.

Since the relation between τ_{del} and τ_{cp} has a direct impact on the TC of the CP, it is useful to consider separately two cases: $\tau_{del} \geq \tau_{cp}$ and $\tau_{del} < \tau_{cp}$, which correspond to the linear and non-linear behaviour of the CP. The switching processes of the CP for both cases are demonstrated in Figs. 4 and 5, respectively [12].

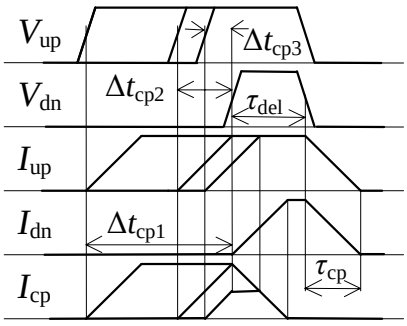

Fig. 4. Charge pump current pulses with control signals at $\tau_{del} \geq \tau_{cp}$.

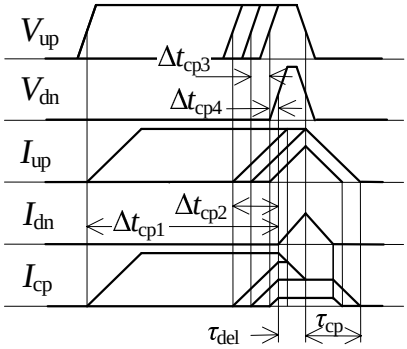

Fig. 5. Charge pump current pulses with control signals at $\tau_{\text{del}} < \tau_{\text{cp}}$.

Linear TC: $\tau_{\text{del}} \geq \tau_{\text{cp}}$. Three different distinctive cases of $\Delta t_{\text{cp1}}, \Delta t_{\text{cp2}}$, and Δt_{cp3} are shown in Fig. 4, resulting in different shapes of the I_{cp} pulses. However, in all cases, averaging of the I_{cp} yields

$$I_{\text{cp,av}} = I_{\text{n}} \Delta t_{\text{cp}}. \tag{2}$$

Thus, the TC is linear and the transfer gain $K_{\text{cp}} = I_{\text{n}}$ is constant. Therefore, $\tau_{\text{del}} \geq \tau_{\text{cp}}$ is the main condition to obtain this desirable feature. In a practical design, it can be fulfilled by selecting the delay τ_{del} long enough compared with τ_{cp}, or by shortening τ_{cp}.

However, the increase of the τ_{del} leads to an excessive width of minimum CP control pulses and, therefore, to a reduction of the PFD operating range. On the other hand, it is difficult to implement fast enough CP at high frequencies, while an increase of the supply current and parasitic charge transfer often appear. Hence, in some applications, where the perfect linearity of the TC is not required, the case $\tau_{\text{del}} < \tau_{\text{cp}}$ can be more suitable.

Distorted TC: $\tau_{\text{del}} < \tau_{\text{cp}}$. Four distinctive cases of $\Delta t_{\text{cp1}}, \Delta t_{\text{cp2}}$, Δt_{cp3}, and Δt_{cp4} are shown in Fig. 5. Here, two different ranges for $\Delta\tau_{\text{cp}}$ should be considered.

First, let us consider the case $|\Delta t_{\text{cp}}| \geq \tau_{\text{cp}} - \tau_{\text{del}}$. Though the wave-forms of the output current pulses, corresponding to the relative time errors $\Delta t_{\text{cp1}}, \Delta t_{\text{cp2}}$, and Δt_{cp3}, are different (see Fig. 5), averaging of the current yields

$$I_{\text{cp,av}} = I_{\text{n}} \Delta t_{\text{cp}} + \text{sign}(\Delta t_{\text{cp}}) I_{\text{off}}, \tag{3}$$

where the shift current (offset) I_{off} can be expressed as

$$I_{\text{off}} = I_{\text{n}} \tau_{\text{del}} (1 - \tau_{\text{del}} / \tau_{\text{cp}}). \tag{4}$$

According to Eqs. (3) and (4), for this range of the input signal, the TC of the CP is also linear, but has a shift of I_{off}. The maximum shift appears at $\tau_{\text{del}} = \tau_{\text{cp}} / 2$, having the value of $I_{\text{off}} = I_{\text{n}} \tau_{\text{del}} / 2$.

If $\tau_{\text{del}} \to 0$ and $\tau_{\text{del}} \to \tau_{\text{cp}}$, the shift current disappears. The first case corresponds to the maximum, the second one to the minimum width of the non-linear region. The differential gain of the CP (the slope of the line) is $K_{\text{cp}} = I_{\text{n}}$.

Secondly, consider the case $|\Delta t_{\text{cp}}| < \tau_{\text{cp}} - \tau_{\text{del}}$. For the PFD output current, following expression can be obtained after averaging (see the output current wave-form for Δt_{cp4} in Fig. 5):

$$I_{\text{cp, av}} = \text{sign}(\Delta t_{\text{cp}}) I_{\text{n}} (\Delta t_{\text{cp}}^2 + 2|\Delta t_{\text{cp}}| \tau_{\text{del}}) / \tau_{\text{cp}}. \tag{5}$$

It follows from Eq. (5) that near zero crossing the TC is non-linear, and the gain of the PFD rises by increasing of the absolute value of the input time difference. At the centre of the non-linear range ($\Delta t_{\text{cp}} = 0$) we have

$$K_{\text{cp}} = \frac{2 I_{\text{n}} \tau_{\text{del}}}{\tau_{\text{cp}}}. \tag{6}$$

Hence, for small values of the ratio $\tau_{\text{del}} / \tau_{\text{cp}}$, the differential gain can be rather small and cause the DZ phenomenon. For $\tau_{\text{del}} = \tau_{\text{cp}} / 2$, the gain equals to the one for the linear part of the TC, while for $\tau_{\text{del}} \to \tau_{\text{cp}}$ the gain equals to the doubled linear gain value. However, since the non-linear region width is close to zero, the TC can be considered as linear.

If $|\Delta t_{\text{cp}}| \to (\tau_{\text{cp}} - \tau_{\text{del}})$, the non-linear curve approaches the linear one, while the differential gain is expressed as $K_{\text{cp}} = 2 I_{\text{n}}$. Hence, the gain value is twice so large as by approaching the critical points at $|\Delta t_{\text{cp}}| = \tau_{\text{cp}} - \tau_{\text{del}}$ from the linear side, and it does not depend on the ratio $\tau_{\text{del}} / \tau_{\text{cp}}$. Thus, the TC is not smooth near the critical value of Δt_{cp} that can cause convergence problems at simulations of complex PLL structures. Some smoothing of the curve may be necessary, which then better corresponds to the real characteristics observed in case of practical implementations.

Some simulated TCs of the CP for different ratios of $\tau_{\text{del}} / \tau_{\text{cp}}$ are shown in Fig. 6 (one half of the curves which are symmetrical with respect to zero point) and Fig. 7 (region near zero crossing). A significant decrease of the gain can be observed at $\tau_{\text{del}} < \tau_{\text{cp}} / 2$. Since the width of the DZ depends on the minimum specified value of the $K_{\text{cp,min}}$, its absolute value can not be determined.

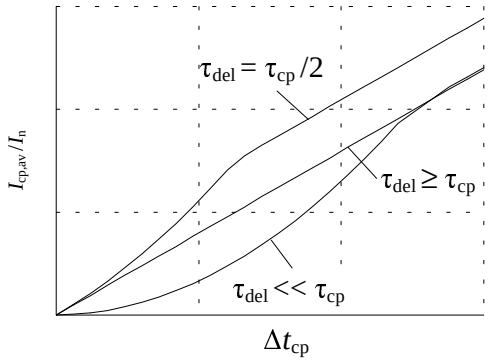

Fig. 6. Transfer characteristic of the charge pump at typical values of the reset delay.

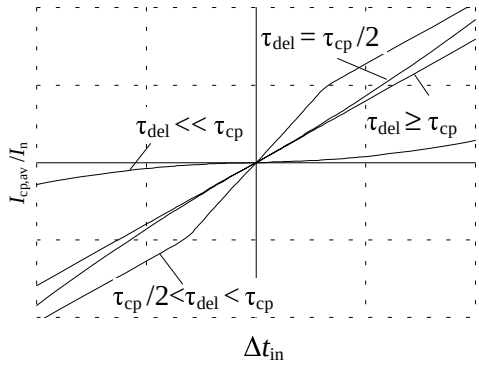

Fig. 7. Transfer characteristic of the charge pump near the zero crossing.

3.2. Non-symmetrical effects

In case of a non-symmetrical CP, the source $(I_{\mathrm{up,n}})$ and sink $(I_{\mathrm{dn,n}})$ currents differ by a value of $\Delta I_{\mathrm{cp}} = I_{\mathrm{up,n}} - I_{\mathrm{dn,n}}$, having different transient times τ_{up} and τ_{dn}, respectively. Then, non-compensated bipolar current pulses appear at the CP output and the TC is distorted even when $\tau_{\mathrm{del}} > \tau_{\mathrm{cp}}$, while the expressions for the $I_{\mathrm{cp,av}}$ are more complicated.

Particularly, supposing that $\tau_{\mathrm{del}} \geq \max(\tau_{\mathrm{up}}, \tau_{\mathrm{dn}})$, and the slew rates for source $(I_{\mathrm{up,n}}/\tau_{\mathrm{up}})$ and sink $(I_{\mathrm{dn,n}}/\tau_{\mathrm{dn}})$ are equal, we obtain

$$I_{\mathrm{cp,av}} = \begin{cases} I_{\mathrm{up,n}} \Delta t_{\mathrm{cp}} + \Delta I_{\mathrm{cp}} \tau_{\mathrm{del}}, & \text{for } \Delta t_{\mathrm{cp}} > 0, \\ I_{\mathrm{dn,n}} \Delta t_{\mathrm{cp}} + \Delta I_{\mathrm{cp}} \tau_{\mathrm{del}}, & \text{for } \Delta t_{\mathrm{cp}} < 0. \end{cases} \tag{7}$$

Increase of the delay τ_{del} causes here a rise of the output offset $\tau_{del}\Delta I_{cp}$, while the module of the gain depends on the sign of the Δt_{cp}.

Normally, the negative effects are negligible at a large enough loop gain, but in some precise applications, the asymmetry of the TC can be important. Hence, the asymmetrical parasitic effects, accounting also for the region of zero crossing, should be mirrored by modelling of the PFD.

4. CONTROL UNIT

4.1. Core structure

Typical implementation of the core structure of a duty cycle insensitive CU is presented in Fig. 8. It is based on NAND gates, though no principal differences in main features follow by using a different logic base. To take into account the proposed modifications [7,10,11,13], delay elements D0, D7, and D8 have been introduced both in the reset and forward paths. The CU is triggered by the falling edge of input signals, while the active state of the output signals is low. In Fig. 8, the V_N represents output signal of the corresponding component GN or DN (N = 0, 1, …, 8).

Modelling of digital structures, especially for high-speed applications, requires an adequate accounting for the gate propagation delay, which depends on several factors. In addition to common dependence on temperature, supply voltage, and particular technology along with schematic and layout solutions of the logic gates, the delay is influenced by the number and loading features of the inputs of following gates. In general, the delay is different for the rise and fall

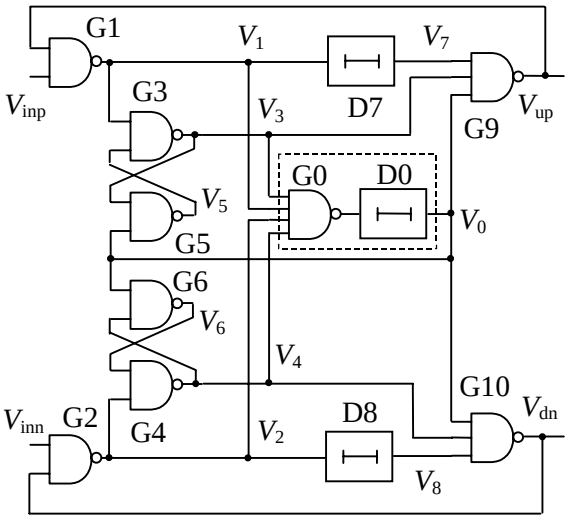

Fig. 8. Typical structure of the control unit.

transitions and even for different inputs of the same gate. A novel method for the delay modelling at sub-micron CMOS structures is presented in [14].

For simplicity, the secondary delay effects are not accounted below, except some particular cases, because of their minor impact due to the symmetrical structure. A simple step approximation of signals is used. Hence, by changing the input state, after the normalized propagation delay a step transition at the output of the Nth component results. Each of the logic components is characterized by its normalized propagation delay τ_{GN} or τ_{DN}, which are assumed to be equal for falling and rising transitions and for symmetrical components of the structure. Thus, *duration of the output pulse of a component cannot be less than the propagation delay*. The delay of D7 and D8 is denoted as τ_1, delay of 2NAND as τ_{21} or τ_{23} (second index denotes the number of output connections of the gate), and delay of 3NAND as τ_3. Total delay of the reset path (components G0 and D0) is denoted as τ_4. Keeping in view the technological background, conditions $\tau_{21} < \tau_{23} < \tau_3 < \tau_4$ have been considered as typical. The parameters of the delay elements are assumed as selectable. As previously stated, the increase of the τ_1 leads to reduction of minimum duration of CU output pulses [13], while increase of the reset delay causes an opposite effect [10,11].

4.2. Conditions for linear transfer characteristic

According to Section 3.1, for a realistic CP with a finite transient time, both control pulses should exist simultaneously during a certain time-period, to achieve a sufficient CP transfer gain near zero crossing. Thus, it is required that

$$\min(t_{up}, t_{dn}) \geq \tau_{cp}. \tag{8}$$

On the other hand, excessive overlapping time of signals reduces the operating phase (time) range of the PFD. Thus, an overlapping time close to τ_{cp} can be considered as optimum.

Let (without loss of generality) $\Delta t_{in} > 0$. The corresponding CU signal timing diagram at $\Delta t_{in} > \tau_4$ is shown in Fig. 9, where t_{mk} $(m = 0, 1, ...;\ k = 0, 1, ...)$ are the transition instants of signals. Here, t_{m0} corresponds to the *m*th transition of the input signals V_{inp} and V_{inn}, and $k > 0$ is the number of sequential transitions of other (internal and output) signals in the interval $t_{m0} < t_{mk} < t_{(m+1)0}$. The respective expressions for transition instants are presented in Table 1.

To generate both the V_{up} and V_{dn} pulses, the transition t_{13} must precede the reset activating at t_{14} $(t_{13} < t_{14}$, Fig. 9). This condition leads to (see expressions for t_{13} and t_{14} in Table 1)

$$\tau_1 < \tau_4 - \tau_3. \tag{9}$$

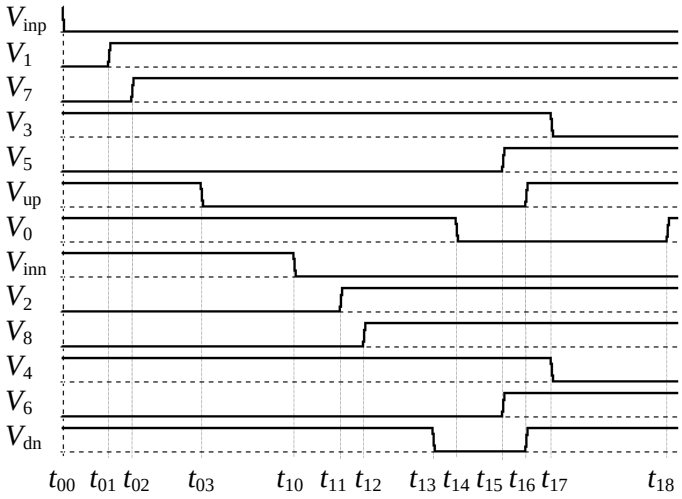

Fig. 9. Control unit signal timing by activating the input.

The duration of the respective output pulses are: $t_{up} = t_{16} - t_{03} = |\Delta t_{in}| + \tau_4 - \tau_1$; $t_{dn} = t_{16} - t_{13} = \tau_4 - \tau_1$, while

$$\Delta t_{cp} = t_{up} - t_{dn} = \Delta t_{in}. \tag{10}$$

Hence, the TC is linear (Fig. 10, line *a*).

Since (according to Section 3.1) the output pulse of the CU cannot be less than τ_3, expressions (8) and (9) yield for an optimal TC

$$\tau_4 - \tau_1 > \max(\tau_{cp}, \tau_3). \tag{11}$$

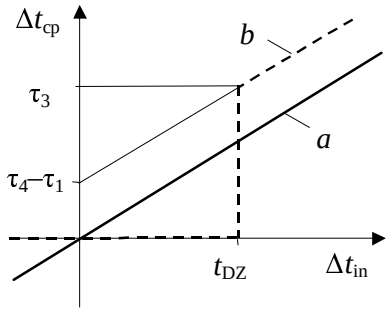

Fig. 10. Approximated transfer characteristic of the control unit.

Table 1. Transition delays by activating the input

t	Delay with respect to t_{00}
t_{00}	0
t_{01}	$\tau_{G1} = \tau_{23}$
t_{02}	$\tau_{G1} + \tau_{D7} = \tau_{23} + \tau_1$
t_{03}	$\tau_{G1} + \tau_{D7} + \tau_{G9} = \tau_{23} + \tau_1 + \tau_3$
t_{10}	$\left\|\Delta t_{in}\right\|$
t_{11}	$t_{10} + \tau_{G2} = \left\|\Delta t_{in}\right\| + \tau_{23}$
t_{12}	$t_{10} + \tau_{G2} + \tau_{D8} = \left\|\Delta t_{in}\right\| + \tau_{23} + \tau_1$
t_{13}	$t_{10} + \tau_{G2} + \tau_{D8} + \tau_{G10} = \left\|\Delta t_{in}\right\| + \tau_{23} + \tau_1 + \tau_3$
t_{14}	$t_{10} + \tau_{G2} + \tau_{G0} = \left\|\Delta t_{in}\right\| + \tau_{23} + \tau_4$
t_{15}	$t_{10} + \tau_{G2} + \tau_{G0} + \tau_{G5(G6)} = \left\|\Delta t_{in}\right\| + \tau_{23} + \tau_{21} + \tau_4$
t_{16}	$t_{10} + \tau_{G2} + \tau_{G0} + \tau_{G9(G10)} = \left\|\Delta t_{in}\right\| + \tau_{23} + \tau_4 + \tau_3$
t_{17}	$t_{10} + \tau_{G2} + \tau_{G5(G6)} + \tau_{G3(G4)} = \left\|\Delta t_{in}\right\| + 2\tau_{23} + \tau_{21}$
t_{18}	$t_{10} + \tau_{G2} + \tau_{G0} + \tau_{G5(G6)} + \tau_{G3(G4)} + \tau_{G0} = \left\|\Delta t_{in}\right\| + 2\tau_{23} + \tau_{21} + 2\tau_4$

For improving the PFD performance, the difference $\tau_4 - \tau_1$ should be equal to τ_{cp} or not much exceed it. For a relatively large τ_4, proper selection of τ_1 permits generation of the output pulses with an optimum duration, close to τ_{cp}. However, a large value of the τ_4 may cause a substantial reduction and shift of the linear region by $\Delta t_{TC} = 2(\tau_{21} + \tau_4)$ (Fig. 11).

Better result can be achieved by selecting the delay τ_4, if its minimum value can be made close enough to $\max(\tau_{cp}, \tau_3)$. Then, the reduction of the linear range will be minimum.

Hence, an optimum selection of the delays would be: $\tau_1 = 0$, $\tau_{21} < \tau_{23} < \tau_3 < \tau_4 \approx \tau_{cp}$.

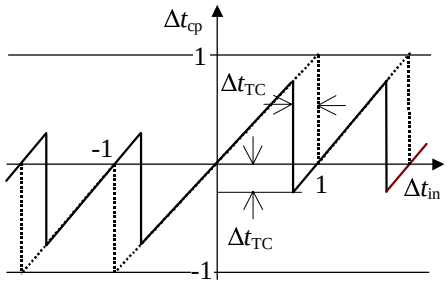

Fig. 11. Approximated transfer characteristic of the ideal (dashed line) and actual (solid line) control unit.

4.3. Reasons of non-linearity and non-stability

In case of $\tau_1 \geq \tau_4 - \tau_3$, the sequence of internal transitions and the character of the function $\Delta t_{cp} = f_{CU}(\Delta t_{in})$ change. A DZ appears near zero crossing, with a range of $\pm t_{DZ}$:

$$t_{DZ} = \tau_1 + \tau_3 - \tau_4. \tag{12}$$

At $|\Delta t_{in}| > t_{DZ}$, the instant t_{14} precedes the t_{13}, and only the V_{up} pulse will be generated. At $|\Delta t_{in}| \leq t_{DZ}$, a sequence $t_{03} \geq t_{14}$ appears, and both the signals V_{up} and V_{dn} are missing. Hence, we have $\Delta t_{cp} = 0$ for $|\Delta t_{in}| \leq t_{DZ}$, and $\Delta t_{cp} = \text{sign}(\Delta t_{in})(|\Delta t_{in}| + \tau_4 - \tau_1)$ for $|\Delta t_{in}| > t_{DZ}$. The corresponding approximated TC is shown in Fig. 10 (line *b*).

Also, an excessive τ_1 may change the normal resetting sequence $t_{20} < t_{22} < t_{23} < t_{30} < t_{32} < t_{33}$ (Fig. 12) of internal transitions during the passive state of the input signal ($t_{20} \leq t < t_{00} + T$). If $\tau_1 > \tau_{23} + \tau_3$, then the abnormal transition sequence of the signals V_7 (V_8) and V_3 (V_4) appears after the deactivation of the CU input signals. It causes generation of the parasitic output pulses with a duration of $t'_{up} = t'_{dn} = \tau_1 - \tau_{23}$.

It can be shown, that if the τ_1 exceeds the value of $\tau_4 + \tau_{23} + \tau_{21}$, additional parasitic pulses appear, and finally an oscillation covers all the passive part of the period (Fig. 13).

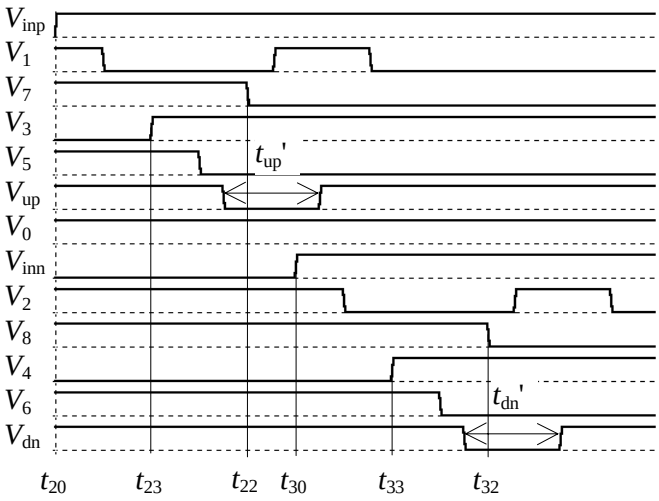

Fig. 12. Parasitic pulses at input resetting $(\tau_1 > \tau_{G3} + \tau_{G9})$.

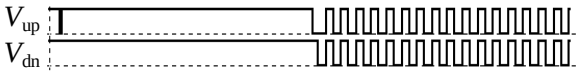

Fig. 13. Oscillating by input resetting $\tau_1 > \tau_4 + \tau_{23} + \tau_{21}$.

4.4. Results of the SPICE simulation

To verify the relationships derived above and to account more precisely for the dynamic behaviour of the logic components, transistor level SPICE simulations of the CMOS based CU were performed. The delay elements were implemented by means of a pair of logic inverters, while variation of delays was achieved by selecting the channel length of transistors. Some simulated waveforms of input (V_{inp}, V_{inn}) and output $(V_q, V_{xq}$ direct, V_{qq}, V_{xqq} buffered by a pair of inverters) signals are presented in Fig. 14 at $\Delta t_{in} T = 10$ ns.

Figure 15 demonstrates the shift of TC at $\tau_1 = 0$ (curve *a*) and $\tau_1 > \tau_4 - \tau_3$ (DZ case, curve *b*), while the calculated $\Delta t_{TC} \approx 0.2$.

The zero crossing region of the TC is shown in Fig. 16, where curve *a* $(\tau_1 = 0)$ has an offset approximately $+0.008$ at $\Delta t_{in} = 0$ and the curve *b* has a DZ in the range of $t_{DC} \approx \pm 0.03$. Also, parasitic oscillations were observed at the derived above conditions.

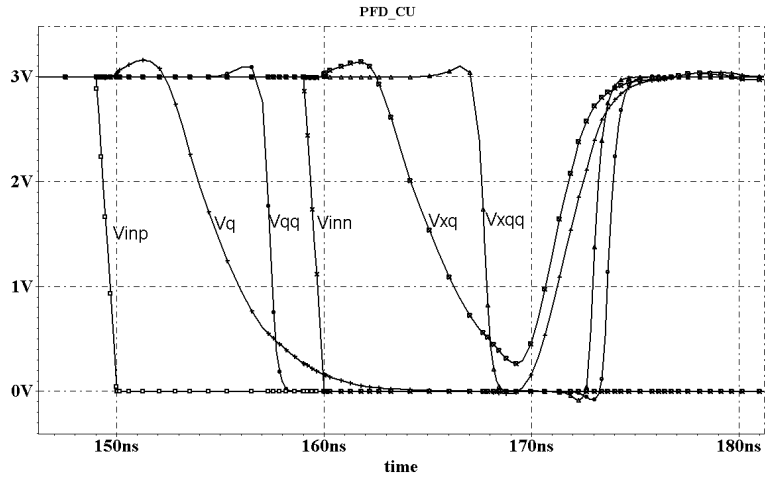

Fig. 14. Simulated signals of the control unit by $\Delta t_{\text{in}}T$ = 10 ns.

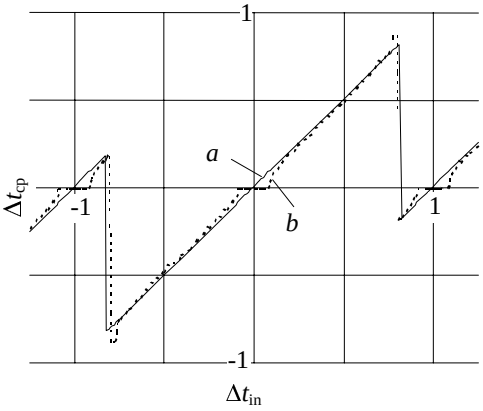

Fig. 15. Transfer characteristics of the control unit (SPICE simulation): $\tau_1 = 0$ (curve *a*); $\tau_1 \geq \tau_4 - \tau_3$ (curve *b*).

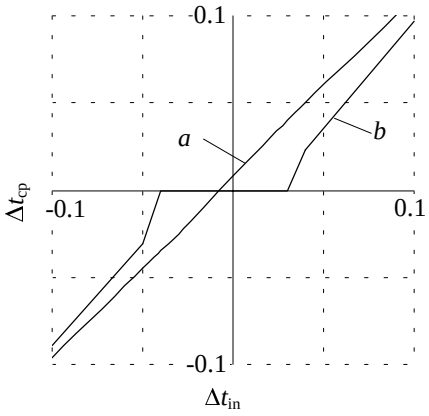

Fig. 16. Transfer characteristic at zero crossing (SPICE simulation): $\tau_1 < \tau_4 - \tau_3$ (curve *a*); $\tau_1 \geq \tau_4 - \tau_3$ (curve *b*).

In general, simulations prove the validity of propositions made above. However, some second-order effects, such as an offset of the TC curves due to asymmetry of the actual transistor-level structure, as well as a small deviation from the linear behaviour near zero crossing and at the ends of the linear range, should be accounted for a more precise modelling of the TC.

5. CONCLUSIONS

The phase frequency detector represents an important functional block of the PLL structure, particularly of the frequency synthesizer. It often consists of two functional blocks – the logic control unit and the charge pump. Converting the time delay between two periodic input signals (and difference of their frequencies) into the analogue signal (average value of the input voltage or current), it ensures perfect control of the whole PLL.

Analysis of the static and dynamic features of a class of PFD, including the CU and CP, was accomplished, in order to explain and model the transfer characteristic in case of typical non-ideal components (delays, inaccuracy, asymmetry). It was shown that the reasons of non-linearity of the PFD transfer characteristic are buried in dynamic behaviour of both the CP and CU.

An insufficient slew rate of the CP, causing relatively long switching times in comparison with the duration of the output signals of the CU, was found to be the main reason for the non-linearity of the CP transfer characteristic, particularly, for the dead zone near the zero crossing. Analytical formulae of the TC were derived for different regions of the input signal, and the minimum width of the CU control signal was found ensuring a linear TC of the CP.

Using the step approximation of signals, an optimum distribution of the component delays for the logic CU was determined, which ensures forming of control pulses with a prescribed minimum width, accounting for the dynamics of the CP. To achieve a linear TC, adjustable delay elements both in forward and feedback paths can be used. However, adjusting the distribution of delays by means of the feedback path, delay maintains maximum linear range of the TC.

In addition, the impact of an asymmetry between the current source and sink of the CP, and some critical aspects at selecting component delays for the CU, leading to the parasitic oscillation, have been considered.

The results of the CU analysis were verified by transistor level SPICE simulation.

The results of the analysis allow macro-modelling of the PFD for fast simulation of processes in different PLL structures.

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FAASISAGEDUSDETEKTORITE LINEAARSUSPIIRANGUD

Vello MÄNNAMA ja Toivo PAAVLE

On analüüsitud ja modelleeritud klassikalisele struktuurile tuginevat laengupumba tüüpi faasisagedusdetektorit, pidades silmas faasilukksüsteemi simuleerimise vajadusi. Faasisagedusdetektori ülekandekarakteristiku mittelineaarsus võib olla tingitud detektori mõlemast funktsionaalsest sõlmest – laengupumbast ja juhtplokist. Laengupumba vooluimpulsside piiratud kasvukiirus kui üks mittelineaarsuse peapõhjustajaid määrab juhtploki väljundimpulsside minimaalse kestuse. Juhtploki üldistatud struktuuri analüüsile tuginedes on esitatud selle komponentide viiviste sobiv kombinatsioon. On vaadeldud ka viiviste valiku kriitilisi aspekte, mis võivad viia ülekandekarakteristiku mittelineaarsusele koos nn. surnud tsooni tekkimisega ja isegi faasisagedusdetektori parasiitsele genereerimisele. Võrdluseks on toodud SPICE simulaatori abil transistortasandil saadud tulemused.