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DEVIATION EXTENSION PROBLEMS AND NONLINEAR EFFECTS IN THE PHASE LOCKED LOOP FREQUENCY DEMODULATORS

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Abstract. In this paper, possibilities for deviation extension of the phase locked loop (PLL) frequency demodulators are considered and some specific features of the PLL systems are analysed. First, optimization of the 3rd order PLL is used in order to reduce substantially the dynamic phase error; that enables the extension of the deviation range. Both theoretical analysis and computer simulation are used to determine the reliable operation limits of the frequency deviation. Second, implementation of the first order PLL as a wideband frequency demodulator is analysed, assuming an effective out-loop postprocessing (filtering) of the output signal. It is shown that the deviation range may be extended almost to the maximum theoretical value, determined by the sampling theorem. Finally, two special periodic signal waveforms, generated in the first order PLL due to the in-loop noise (ripple), are demonstrated and analysed.

Key words: phase locked loop, frequency demodulator, frequency deviation, dynamic phase error, filter optimization, computer simulation, signal distortion.

1. INTRODUCTION

Demodulation of frequency modulated (FM) signals is one of the most important implementations of the PLL. Deviation extension makes it possible to improve the signal-to-noise ratio and to lower the demodulation threshold.

At the 70 MHz intermediate frequency, extension of the deviation range up to 18 MHz and even more is desirable for the 10 MHz signal bandwidth (BW).

However, problems arise when applying the conventional PLL frequency demodulators (FDEM) in case of FM signals with extended deviation, because the dynamic phase error (DPE) in the PLL exceeds the critical level. Therefore the output signal is heavily distorted and the PLL can even drop out of lock. The other restriction is the limited frequency control range of the voltage-controlled oscillator (VCO).

Classical structure of a PLL FDEM is shown in Fig. 1 [1–3]. It consists of a phase detector (PD), a low-pass filter (LPF), and a VCO, forming a feedback control system. The input signal is characterized by the phase Θ_i and the frequency f_c of the carrier, the corresponding parameters of the VCO are denoted as Θ_o and f_o. The closed loop transfer function of the linear structure can be expressed as

$$H(s)=\frac{V_{out}(s)}{\Delta f_i(s)}=2\pi\frac{K_d F(s)}{s+K_d K_o F(s)}, \tag{1}$$

where V_{out} is the output voltage, Δf_i is the input frequency deviation, and $F(s)$ is the transfer function of the LPF. The gains of the PD and VCO are denoted as K_d [V/rad] and K_o [rad/(s V)], respectively. Often the open loop transfer coefficient (velocity gain) $K_v = K_d K_o$ [rad/s] is used. That corresponds to the hold range of the PLL without the LPF, which means that $F(s)=1$.

For the stepwise frequency deviation $\Delta f_i = \Delta\omega_i/2\pi$, the steady state phase error $\Theta_e = \Theta_i - \Theta_o$ can be expressed as

$$\Theta_e(t\to\infty)=\arcsin\left(2\pi\frac{\Delta f_i}{K_d K_o}\right), \tag{2}$$

while the steady state output voltage is

$$V_{out}=2\pi\frac{\Delta f_i}{K_o}. \tag{3}$$

According to (2), the largest static frequency deviation, max $\Delta f_i \le K_v/2\pi$, corresponds to the phase error $\Theta_e = 90°$. The actual deviation value must be several times smaller, because the DPE can considerably exceed the static value.

The output voltage in Eq. (3) is reciprocal to K_o. Thus, the nonlinear distortion of the output signal is directly related to the nonlinearity of the VCO's transfer characteristic within the signal BW.

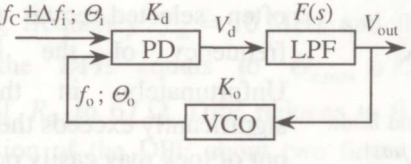

Fig. 1. Classical PLL FDEM.

The transfer function of the multiplying PD has a sine form nonlinearity, and the output voltage V_d of the PD is unavoidably accompanied by the double input frequency ripple. Assuming that the ripple is totally suppressed by the LPF, the output voltage of the PD is expressed as

$$V_d = A_i A_o G_d \sin\Theta_e, \tag{4}$$

where A_i is the input voltage amplitude, A_o is the VCO's voltage amplitude, and G_d is the electronic gain of the PD. Altogether they form the gain $K_d = A_i A_o G_d$ [V/rad] of the PD.

However, in some cases LPF may disturb the demodulation process and retard dynamics of the PLL.

The LPF in the 3rd order PLL is usually a 2nd order RC filter [4–7] with the transfer function

$$F(s) = \frac{\omega_{p1}\omega_{p2}(s+\omega_z)}{\omega_z(s+\omega_{p1})(s+\omega_{p2})}, \tag{5}$$

where $\omega_{p1} = 2\pi f_{p1}$, $\omega_{p2} = 2\pi f_{p2}$, and $\omega_z = 2\pi f_z$ correspond to the characteristic frequencies of the LPF. The Bode plots of the $F(s)$ and the open loop transfer function $H_o(s) = K_v F(s)/s$ of the PLL linear model are shown in Fig. 2. The structure of the LPF is also shown.

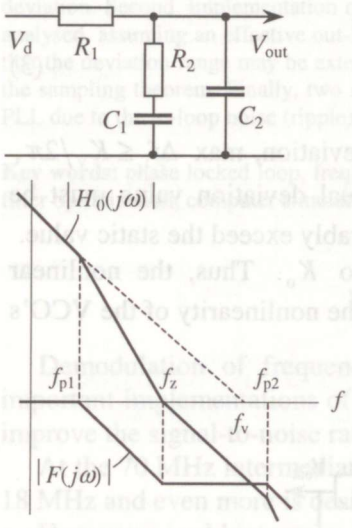

Fig. 2. The 2nd order LPF and Bode plots of $|F(j\omega)|$ and $|H_o(j\omega)|$.

Typically, $R_1 >> R_2$ and $C_1 << C_2$ are chosen, and thus, $f_{p1} << f_z << f_{p2}$. For example, the classical demodulator based on the IC NE568 [K_d = 0.127 V/rad, $K_o = 4.2 \times 10^9$ rad/(s V), $f_v = K_v/2\pi$ = 84.9 MHz] has the following recommended values of the LPF components [6]: R_1 = 200 Ω (internal resistance), R_2 = 27 Ω, C_1 = 56 pF, C_2 = 560 pF. Hence, f_{p1} = 1.16 MHz, f_z = 10.5 MHz, and f_{p2} = 129 MHz.

In order to minimize the noise BW, f_z is often selected equal to the zero crossing frequency of the $|H_o(j\omega)|$ plot [5]. Unfortunately, in this case the DPE significantly exceeds the static error and a drop out of lock may easily occur.

2. PARAMETRIC OPTIMIZATION OF THE LPF

For the 3rd order PLL, analytical formulae to determine the dynamic parameters are rather complicated or lacking. Due to the sufficient difference of the frequencies f_z and f_{p2}, the latter can be taken as infinity ($C_1 = 0$), and a second order PLL results. Then the maximum DPE, corresponding to the case of sine wave modulation with the frequency of the PLL's natural frequency $f_n = \sqrt{K_v C_2 (R_1 + R_2)} / 2\pi$, can be expressed as

$$\Theta_{e,max} \cong \Delta f_i / (2\xi f_n), \tag{6}$$

where $\xi = f_n / (2 f_z)$ is the damping factor of the $H(j\omega)$ for $C_1 = 0$. The approximate expressions for the lock-in range is

$$\Delta f_L \cong 2\xi f_n = f_n^2 / f_z, \tag{7}$$

and the pull-in time

$$T_P \cong (\Delta f_i)^2 / (4\pi\xi f_n^3) \tag{8}$$

can also be used for estimating the respective parameters of the 3rd order PLL FDEM [2].

One possible way for reduction of the DPE is shifting the zero-crossing frequency (Fig. 2) approximately into the middle of f_z and f_{p2} [7]. According to the analysis of Eq. (1) and computer simulations, the value of R_2 is the most appropriate parameter for the LPF for this tuning (Fig. 2). Simulation of $H_o(j\omega)$ for a number of values of R_2 clearly demonstrates that due to the change of R_2 from 27 to 87 Ω, the phase margin significantly increases [8]. It has a direct impact on the dynamic properties of the closed loop system and leads to a rapid decrease of the DPE.

As an illustration, let us consider again the particular case of the PLL FDEM discussed above. For the recommended (original) value of R_2 = 27 Ω, the maximum value of the DPE at the frequency step of Δf_i = 18 MHz is approximately 1.1 rad. Increasing R_2 to 67 Ω reduces this value by 1.4 times. Even more critical is the situation in case of sine wave modulation. For example, having the modulating frequency f_m = 10 MHz and the maximum deviation max Δf_i = 18 MHz, the DPE equals to $\Theta_{e,max} \cong 1.8$ rad at R_2 = 27 Ω. Increasing the value of R_2 to 67 Ω, DPE reduces to 0.95 rad [8,9]. Hence, an easily achieved reduction of the DPE about two times lowers its level safely below the critical one.

Further increase of R_2 is less effective, because some negative effects appear simultaneously. Due to the reduction of suppression of the second harmonic

component of the carrier, the ripple of the VCO's input signal increases (especially at the minimum ripple frequency, which is 2(70–18) = 104 MHz in our case), and also an increase of the noise BW can be noticed.

According to simulations, the first effect is almost negligible and it can be simply compensated using an additional output filter outside the loop. For the noise BW estimations, the following approximate formula is often used for the second order PLL ($C_1 = 0$) [2]:

$$B_L = \int_0^\infty (|H(j\omega)|)^2 \mathrm{d}\omega \cong \pi f_n (\xi + 1/\xi). \tag{9}$$

In general, however, this simple expression is not directly suitable for the 3rd order PLL. A more complicated but exact formula for the noise BW of the third order PLL is presented in [7]:

$$B_L = \frac{\pi f_n (1 + h + 1/(\nu\mu))}{2(1 + 1/(h\mu) - (1 - 1/\mu + 1/(h\mu^2))/\nu)}, \tag{10}$$

where $\mu = f_z / f_{p1}$, $\nu = f_{p2} / f_z$, and $h = (f_n f_{p1}) / f_z^2$ (Fig. 2).

Increase of the noise BW due to the increase of R_2 from 27 to 67 Ω is relatively small, approximately 23%. However, further increase of R_2 causes an accelerating increase of the noise BW. Thus, the reasonable value of R_2 is approximately between 60 and 70 Ω.

The values of the lock-in range Δf_L and pull-in time T_P have been also estimated using Eqs. (7) and (8), respectively. The initial values at R_2 = 27 Ω are Δf_L = 10 MHz and T_P = 43 ns, while at R_2 = 67 Ω these values change to Δf_L = 21 MHz and T_P = 26 ns. Improvement of these important dynamic parameters is obvious.

3. IMPACT OF THE PD NONLINEARITY

For the investigation of various nonlinear effects in the PLL FDEM, an original computer simulation program has been developed. Particularly, the nonlinear behavior of the PD is taken into account. Next, some results of simulation of the particular PLL FDEM, discussed above, are presented.

A response to the frequency step Δf_i = 18 MHz is shown in Fig. 3 in case of different values of R_2 (without taking into account the ripple at the PD output).

Simulated closed loop signals at the input sine wave modulation are shown in Fig. 4a (R_2 = 27 Ω) and 4b (R_2 = 67 Ω), where $\Delta f_0 = f_i(t) - f_0(t) = \Delta f_i(t) - K_o V_{out}(t)$ is the instantaneous value of the virtual frequency difference.

In the case (a) the signal is irregular, because the demodulator drops out of lock. In the case (b) the behaviour of the system is regular. Thus, the desired level of the DPE is obtained to get safe operation of the PLL FDEM.

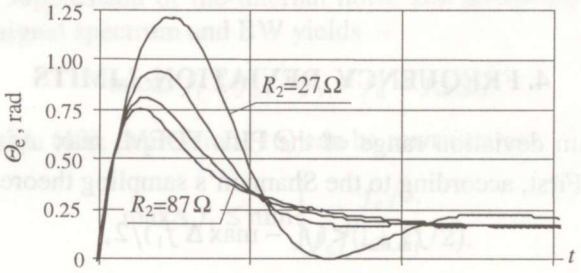

Fig. 3. Step response ($\Delta f_i = 18$ MHz) at $R_2 = 27$ to 87 Ω (step 20 Ω).

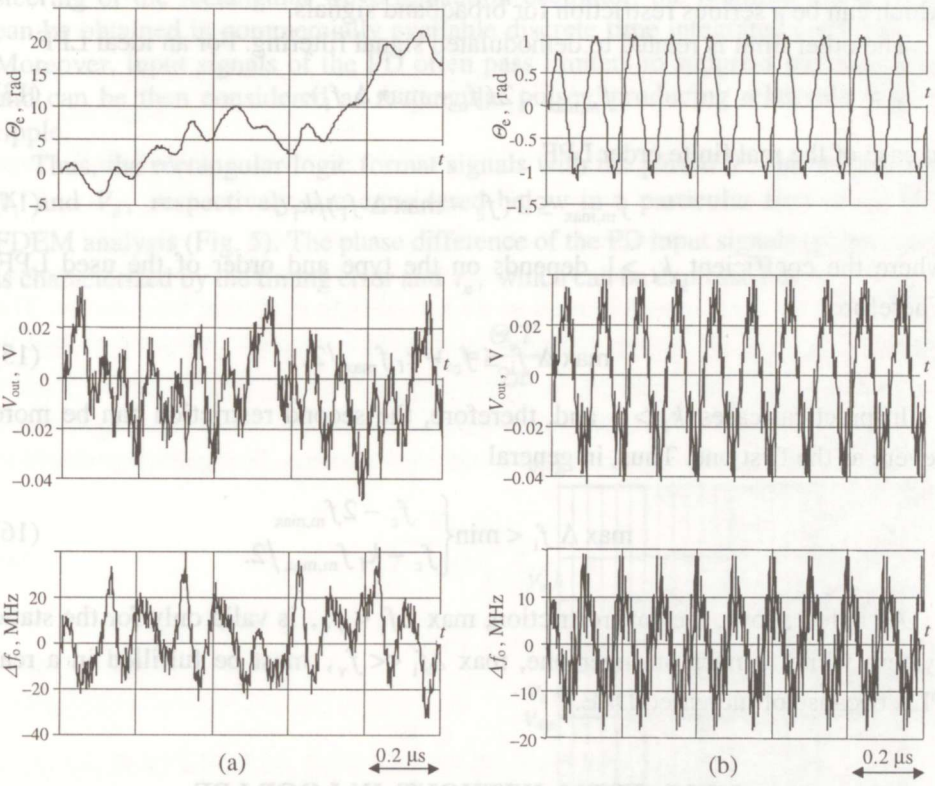

Fig. 4. Simulated waveforms of the Θ_e, V_{out}, and Δf_o at sine wave modulation of the input signal ($f_m = 10$ MHz, max $\Delta f_i = 18$ MHz): (a) $R_2 = 27$ Ω, (b) $R_2 = 67$ Ω.

Comparing the results with linear analysis (Section 2), a difference between the DPE peak values can be noticed, which is caused by the sinusoidal character of the PD. To guarantee the same level of the control voltage at the VCO input as in the linear case, a greater phase difference appears between the PD inputs.

4. FREQUENCY DEVIATION LIMITS

The maximum deviation range of the PLL FDEM, max Δf_i, is limited by several factors. First, according to the Shannon's sampling theorem

$$f_{m,max} < (f_c - \max \Delta f_i)/2, \tag{11}$$

where $f_{m,max}$ is the maximum modulation frequency and f_c is the center (carrier) frequency. Thus,

$$\max \Delta f_i < (f_c - 2f_{m,max}), \tag{12}$$

which can be a serious restriction for broadband signals.

The other limit is related to demodulated signal filtering. For an ideal LPF

$$f_{m,max} < 2(f_c - \max \Delta f_i). \tag{13}$$

In case of the real finite order LPF

$$f_{m,max} \leq 2(f_c - \max \Delta f_i)/k_f, \tag{14}$$

where the coefficient $k_f > 1$ depends on the type and order of the used LPF. Therefore,

$$\max \Delta f_i \leq f_c - k_f f_{max}/2. \tag{15}$$

In practical cases $k_f > 4$ and, therefore, the second restriction can be more severe as the first one. Thus, in general

$$\max \Delta f_i < \min \begin{cases} f_c - 2f_{m,max} \\ f_c - k_f f_{m,max}/2. \end{cases} \tag{16}$$

As noted above, the soft restriction, max $\Delta f_i < f_v$, is valid only for the static system while a much stronger one, max $\Delta f_i << f_v$, must be fulfilled in a real PLL because of increased DPE.

5. PLL FDEM WITHOUT IN-LOOP LPF

The maximum overshoot of the DPE, which significantly reduces the input frequency deviation range, rapidly increases with the order of the PLL. Let us consider now a particular case of the first order PLL FDEM without the in-loop

LPF, instead of which an external postprocessing filter is used. The corresponding PLL has a flat frequency response without overshoot, with the cut-off frequency f_h which is equal to f_v (Fig. 2). The broad BW of this PLL maintains good suppression of the internal noise and disturbance [10,11]. Fitting the modulating signal spectrum and BW yields

$$\max\Delta f_i \le f_v, \quad f_v = f_h = f_{m,\max}, \tag{17}$$

and using condition (13), expression (16) can be rewritten as

$$\max\Delta f_i \le \min\begin{cases} f_c/3, \\ f_c/(1+k_f/2). \end{cases} \tag{18}$$

In order to achieve the maximum deviation range in the first order PLL FDEM, a VCO or current controlled oscillator (CCO) with a wide linear range is necessary, first of all because of a large double frequency ripple in the case of sine wave input signals of the PD (Section 6). However, using current-mode steering of the rectangular wave relaxation oscillator, the required linear range can be obtained in commercially available discrete time integrated circuit PLLs. Moreover, input signals of the PD often pass limiters to suppress parasitic AM, and can be then considered as rectangular pulses, producing relatively smaller ripple.

Thus, the rectangular logic format signals with the period T and magnitudes V_i and V_o, respectively, are considered below in a particular first order PLL FDEM analysis (Fig. 5). The phase difference of the PD input signals (phase error) is characterized by the timing error and t_e, which can be expressed as

$$t_e = \frac{\Theta_e T}{2\pi}. \tag{19}$$

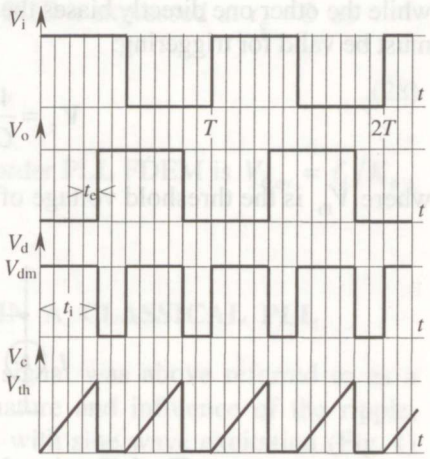

Fig. 5. Waveforms of the PD voltages V_i, V_o, and V_d, and the voltage V_c across the VCO timing capacitance.

Using the XOR logic gate as the PD, the regular range of t_e is

$$-\frac{T}{4} < t_e < \frac{T}{4}. \tag{20}$$

The output voltage of the PD is a sequence of rectangular pulses:

$$V_d = \begin{cases} V_{dm}, \text{ if } n\frac{T}{2} \le t < (2n+1)\frac{T}{4} + t_e, \\ 0, \text{ if } (2n+1)\frac{T}{4} + t_e \le t < (n+1)\frac{T}{2}, \ n = 0, 1, 2, ..., \end{cases} \tag{21}$$

having average value

$$V_{d,av} = \frac{2}{T}\int_0^{T/2} V_d \, dt = \frac{V_{dm}}{2} + 2\frac{t_e}{T}V_{dm}. \tag{22}$$

Thus, at zero phase error ($t_e = 0$) we obtain $V_{d,av} = V_{dm}/2$, and transfer gain of the PD is

$$K_d = \frac{\Delta V_{d,av}}{\Delta \Theta_e} = \frac{V_{dm}}{\pi}. \tag{23}$$

Often the VCO contains a CCO having a linear gain and a wide frequency range [3], and a voltage-to-current converter having the transconductance G_m.

Let us consider implementation of the rectangular wave VCO by a transconductance circuit and a symmetrical emitter-coupled (source-coupled) multivibrator, which is widely used as a CCO at high operating frequencies. The charge process of the timing capacitor is explained using the structure shown in Fig. 6 where the control current I_c is mirrored through two identical sources. The voltage drop V_c across the timing capacitor C is caused by one of the two sources, while the other one directly biases the switching transistor. The following condition must be valid for triggering:

$$V_c = \frac{1}{C}\int_0^{T/2} I_c \, dt = V_{th}, \tag{24}$$

where V_{th} is the threshold voltage of the CCO.

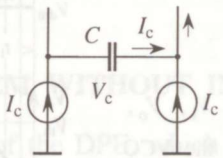

Fig. 6. Charging of the timing capacitor of CCO.

Considering the classical PLL FDEM structure where the PD average signal $V_{d,av}$ is available, and replacing I_c in (24) by $V_{d,av}G_m$, we obtain

$$f_o = \frac{1}{T} = V_{d,av}K_o, \qquad K_o = \frac{G_m}{2CV_{th}}. \tag{25}$$

For the PLL FDEM without internal LPF one can utilize the timing capacitor C in the CCO for averaging the PD output signal. Replacing I_c in (24) by $V_d G_m$, yields

$$t_i = \frac{T}{4} + t_e = \frac{V_{th}C}{V_{dm}G_m} = \frac{1}{2V_{dm}K_o}. \tag{26}$$

According to Eq. (26), the value of t_i (pulse width of the PD output signal) is determined by the internal parameters of the demodulator and it does not depend on the input signal deviation. The value of t_i can be changed by selecting the control current (which determines the value of G_m), the capacitance of the timing capacitor C, or the values of V_{th} and V_{dm}.

The timing error t_e is directly influenced by changes in the input signal period.

The slope of V_c is:

$$\frac{dV_c}{dt} = \frac{V_{dm}G_m}{C}. \tag{27}$$

The pulse width t_i of the PD output signal determines the minimal (semi)period of the CCO and the maximal deviation range of the input frequency, while the minimal operating frequency can be selected rather small.

The free-running frequency $f_c = f_o$ of the CCO is expressed at $t_e = 0$ as

$$f_c = \frac{V_{dm}G_m}{4CV_{th}}, \tag{28}$$

while the average output voltage of the first order PLL FDEM is $V_{d,av} = f_i/K_o$, the same as in the general case.

6. WAVEFORM CONVERSION IN A CLASSICAL PLL

The ripple component in the PD output signal was above referred to as a disturbing factor. Now, let us analyse the nature and influence of the ripple, keeping in view the classical first order PLL with sine wave excitation (Fig. 1) [12].

In case of a harmonic input signal $V_i = A_i \sin(\omega_i t)$ without deviation ($\omega_i = \omega_c$), and taking $A_i = A_o = 1$ [Eq. (4)], the closed loop first order PLL can be described with the next system of equations:

$$\begin{aligned} V_d(t) &= V_o(t)\sin(\omega_c t), \\ V_o(t) &= \cos\int[\omega_c + K_o V_d(t)]\,dt. \end{aligned} \tag{29}$$

The system (29) has no analytical solution and can be solved with respect of $V_d(t)$ and $V_o(t)$ only numerically. In order to understand the forming process of the signals and to determine their harmonic composition, it is appropriate to consider this process step by step.

Let us assume for the first step of iteration that the output signal of the PD has only the double-frequency component: $V_d'(t) = \sin(2\omega_i t)$, which serves as the control signal for the VCO. Then, the output signal of the VCO is expressed as:

$$\begin{aligned} V_o(t) &= \cos[\omega_c t - G\cos(2\omega_c t)/2] \\ &= \cos(\omega_c t)\cos[G\cos(2\omega_c t)/2] + \sin(\omega_c t)\sin[G\cos(2\omega_c t)/2], \end{aligned} \tag{30}$$

where $G = K_d K_o/\omega_c = K_v/\omega_c$ is the normalized gain of the loop.

We can transform Eq. (30) as:

$$\begin{aligned} V_o'(t) = \cos(\omega_c t)\left[J_0(G/2) + 2\sum_{k=1}^{\infty}(-1)^k J_{2k}(G/2)\cos(4k\omega_c t)\right] \\ + \sin(\omega_c t)2\sum_{k=1}^{\infty}\left\{(-1)^{k+1} J_{2k-1}(G/2)\cos[2(2k-1)\omega_c t]\right\}, \end{aligned} \tag{31}$$

where J_k is the Bessel function with the index k ($k = 1, 2, \ldots$).

The result of the first iteration of (31) can be written as

$$V_o'(t) = \sum_{k=1}^{\infty} a'_{2k-1}\cos[(2k-1)\omega_c t] + \sum_{k=1}^{\infty} a''_{2k-1}\sin[(2k-1)\omega_c t], \tag{32}$$

where $a'_n = f[J_{n-1}(G/2),\ J_{n+1}(G/2)]$ and $a''_n = f[J_{n-1}(G/2),\ J_{n+1}(G/2)]$, $(n = 1, 2, \ldots, 2k-1)$.

Thus, the double frequency component at the VCO input will induce a complex signal at its output, in which the fundamental component accompanies the infinite sum of higher odd harmonics.

Multiplying now, for the next iteration, V_o' in PD by the input signal $V_i(t)$, we obtain the PD output signal, consisting only of the even harmonics:

$$V_o''(t) = \sum_{k=1}^{\infty} b'_{2k}\sin(2k\omega_c t) + \sum_{k=1}^{\infty} b''_{2k}\cos(2k\omega_c t), \tag{33}$$

where the coefficients b'_n and b''_n $(n=1, 2, \ldots, 2k)$ are also determined by the factor G.

It can be shown that further iterations will specify the values of the coefficients a and b, but will not change the structure of expressions (32) and (33). Consequently, we can express the VCO and PD output signals as Fourier series:

$$V_o(t) = \sum_{k=1}^{\infty} A_{2k-1} \sin[(2k-1)\omega_c t + \Psi_{2k-1}], \tag{34}$$

$$V_d(t) = \sum_{k=1}^{\infty} B_{2k} \sin(2k\omega_c t + \theta_{2k}), \tag{35}$$

where $A_n = fA(G)$ and $\Psi_n = f\Psi(G)$, $(n=1, 3, \ldots, 2k-1)$, denote the magnitude and initial phase of the nth component of the series, respectively, while $B_n = fB(A_{n-1}, \Psi_{n-1}, A_{n+1}, \Psi_{n+1})$ and $\theta_n = f\theta(A_{n-1}, \Psi_{n-1}, A_{n+1}, \Psi_{n+1})$, $(n=2, 4, 6, \ldots, 2k)$.

In general, the input signal frequency can have a deviation $\Delta\omega_i$ in respect to the central frequency. In this case, each amplitude A_n and initial phase Ψ_n of the harmonics are functions of two variables, G and γ, where $\gamma = \Delta\omega_i / K_v$ is the initial relative frequency deviation.

In order to solve the system (29) numerically, a special PLL simulation program was developed. The dependence of the magnitudes of odd harmonics (up to the 15th) of the VCO output signal V_o on G is shown in Fig. 7 at $\Delta\omega_i = 0$, where $\alpha_k = A_k / A_o$ denotes the relative magnitude of the kth component. According to simulations, the waveforms of the V_o are close to sinusoidal in case of $G \ll 1$, and significantly distorted for greater values of G (Fig. 8).

The product of multiplying the input signal to the fundamental component of the VCO output is the only non-zero (averaged) component in the PD output voltage. Thus the value of A_1 is most important, because the PD gain K_d and the loop gain K_v (Section 1) are proportional to it. Consequently, the validity range of the PLL depends on A_1, too.

In Fig. 9, variation of the relative magnitude $\alpha_1 = A_1 / A_o$ of the VCO output as a function of G and γ is shown in case of the input frequency deviation. Discontinuity of the curves at $\gamma = \gamma_{max}$ determines the limit of the synchronization capability (capture range) of the loop.

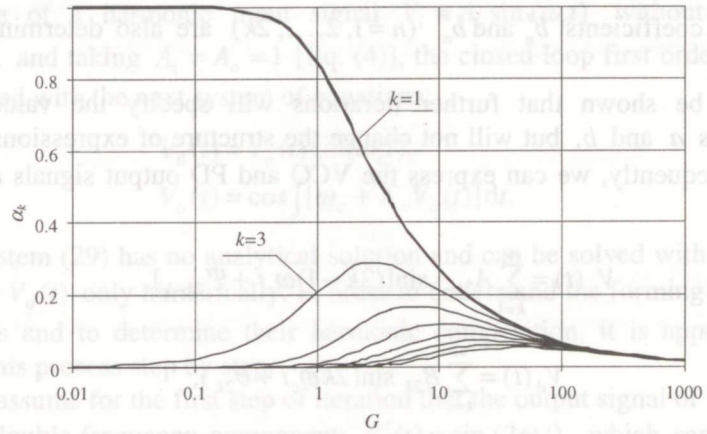

Fig. 7. The magnitudes of the odd harmonics at $\Delta\omega_i = 0$ ($k = 1, 3, ..., 15$).

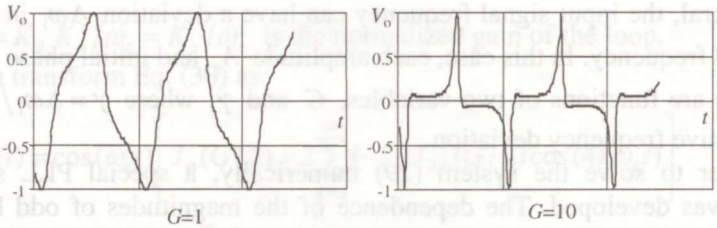

Fig. 8. Output signal of the VCO for different values of the parameter G.

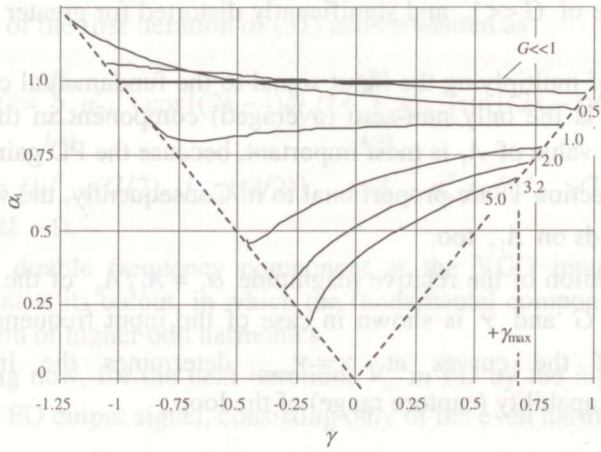

Fig. 9. Normalized magnitude of the main harmonic vs relative deviation γ at various values of the parameter G.

7. CONCLUSIONS

It has been demonstrated that the dynamic phase error of the PLL frequency demodulators can be substantially reduced by optimal selection of the demodulator parameters (particularly, by the low-pass filter tuning), while increase of the noise bandwidth and the ripple at the voltage-controlled oscillator input is not noticeable. As the result, a significant extension of the deviation range for the input signal is obtained.

For example, a reduction of the dynamic phase error up to two times has been achieved in case of a typical monolithic PLL demodulator circuit, while the increase of the noise bandwidth less than 25% has been observed at the 70 MHz centre frequency, 18 MHz deviation range, and 10 MHz signal bandwidth. Theoretical and simulation results have been supported by experiments.

A possibility to use the first order PLL as a frequency demodulator has been analysed. It has been demonstrated that in a PLL without in-loop low-pass filter, the role of the averaging circuit for the phase detector output signal can play the timing capacitor of the current controlled oscillator. Such PLL frequency demodulator may have outstanding linearity and wide bandwidth without dynamic phase error overshoot, which enables an extremely wide frequency deviation of the input signal.

Additionally the impact of the ripple as an unavoidable component of the volatage-controlled oscillator control has been investigated. It has been demonstrated that the ripple can induce a quite large distortion of the oscillator output waveform, primarily generated as sinusoidal. The harmonic composition of the output signals of the phase detector and oscillator was shown to depend on the relative open loop gain and the input frequency deviation.

From the mathematical point of view, the PLL system generates two specific periodic signals, one of which consists of the odd harmonic components, and the other one of even components.

As a result, a way for improving the performance of the PLL frequency demodulators has been achieved in comparison with the classical solutions, while the described theoretical considerations serve for better understanding of complex dynamic processes taking place in the nonlinear PLL systems.

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DEVIATSIOONI LAIENDAMISE PROBLEEMID JA MITTELINEAARSED EFEKTID FAASILUKKSÜSTEEMI SAGEDUSDEMODULAATORITES

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On vaadeldud faasilukksüsteemile (FLS) tuginevate sagedusdemodulaatorite (SDEM) deviatsiooni laiendamise võimalusi, samuti üldisi protsesse esimest järku FLS-s. Kolmandat järku FLS SDEM-i korral võimaldab filtri parameetrite traditsioonilise kombinatsiooni asendamine esitatud optimaalse valikuga tunduvalt vähendada dünaamilist faasiviga ja seetõttu oluliselt laiendada sisendsignaali sagedusdeviatsiooni.

Teise küsimusena on käsitletud esimest järku FLS SDEM-i rakendatavust deviatsioonipiiride avardamiseks, kusjuures eeldatakse, et puuduva süsteemisisese madalpääsfiltri funktsioon on antud erilisele väljundfiltrile. Selline lahendus võimaldaks deviatsiooni suurendada teoreetilise maksimumi lähedale.

Lõpuks on selgitatud korrutava faasidetektori väljundis vältimatult esineva häiresignaali mõju ahelasisestele protsessidele ning demonstreeritud kahe erikujulise perioodilise signaali (funktsiooni) genereerimise võimalust esimest järku FLS-i abil. Teoreetilisele analüüsile on lisatud spetsiaalse, FLS-de analüüsiks loodud arvutisimulaatori abil saadud tulemused.